AMENDMENTS TO THE CLAIMS

1. (Amended) A memory device for performing ~~a~~ at least one self-refresh operation ~~in a self-refresh period instigated for every constant time interval after entering into~~ during a self-refresh mode, comprising:

~~a low-power controller outputting a enable signal for enabling the power supply means during the self-refresh period after being enabled in the self-refresh mode; and~~

a power supply means ~~receiving the enable signal~~ for ~~supplying~~ generating a low and a high voltages, which are used in an internal circuit, according to an enable signal by using an external supply voltage and a ground voltage~~,~~; and

a low-power controller for generating the enable signal according to a performance of the self-refresh operation during the self-refresh mode, wherein the enable signal is activated when the self-refresh operation is performed and is inactivated when the self-refresh operation is not performed,

wherein the low voltage is lower than the ground voltage and the high voltage is higher than the external supply voltage.

2. (Amended) The memory device of claim 1, wherein the power supply means ~~for refreshing stored data during a self-refresh period operated for every predetermined interval after entering into a self-refresh mode~~ includes:

a high power generator for receiving the external supply voltage ~~for supplying~~ to thereby supply the high voltage to the internal circuit~~, the high voltage being higher than the power voltage~~ according to the enable signal; and

a low power generator for receiving the external supply voltage ~~for supplying~~ to thereby supply the low voltage to the internal circuit~~, the low voltage being lower than the ground voltage~~ according to the enable signal.

3. (Original) The memory device of claim 2, wherein the power supply means further includes a normal-power generator for supplying an internal voltage to the internal circuit.

4. (Amended) The memory device of claim 1, wherein the low-power controller includes;

a first NAND gate receiving a self-refresh enable signal ~~enabled in~~ activated during the self-refresh mode and a self-refresh termination signal ~~enabled at a moment of terminating the self-refresh period~~ activated when the self-refresh operation is terminated;

a second NAND gate receiving an output signal of the first NAND gate ~~and an output signal of a third NAND gate~~; and

a third NAND gate receiving an inverted signal of a self-refresh operating signal ~~enabled at a moment of beginning the self-refresh period~~ activated during the self-

refresh operation and an output signal of the second NAND gate, wherein an output signal of the third NAND gate is inputted to the second NAND gate.

5. (Amended) The memory device of claim 3, wherein the high voltage generator includes:

a high voltage sensor for sensing the second power voltage level and being disabled ~~in the self-refresh period~~ when the self-refresh operation is performed;

a generator for generating a clock signal ~~by being controlled by a result sensed by the high voltage sensor~~ according to a sensing result of the high voltage sensor; and

a high voltage generating pump for generating ~~a~~ the high voltage ~~by being controlled by~~ in response to the clock signal.

6. (Amended) A method for operating the memory device, comprising the steps of:

entering into a self-refresh mode; and

~~operating~~ performing ~~a refresh~~ at least one self-refresh operation ~~in a self-refresh period instigated for every constant interval of~~ during the self-refresh mode, wherein a high voltage and a low voltage are generated when the self-refresh operation is performed and are not generated when the self-refresh operation is not performed,

wherein ~~the internal power is supplied during the self-refresh period of the self-refresh mode~~ the high voltage is higher than an external power supply voltage and the lower voltage is lower than a ground voltage.

AMENDMENTS TO THE SPECIFICATION

On page 11, paragraph beginning on page 10 and commencing on page 12, line 2,

As shown, the memory device related to refresh operation includes a DRAM state controller 800, a self-refresh operation controller 700, a generator 600, a frequency divider 500, a self-refresh mode controller 100, a sense-amplifier controller 900, a self-refresh termination controller 950, a cell area 400, a cell controller 200, and a power supply division 300. The memory device further includes a low-power controller 300'. The DRAM state controller 800 controls a state of the memory device, e.g., storing, reading, refreshing, after receiving several control signals such as /RAS, /CAS, /WE, /CS, CKE, CLK, and so on from an external circuit. The self-refresh operation controller 700 outputs a self-refresh enable signal (hereinafter, referred as 'selfref' signal) after receiving a self-refresh entering signal herein, referred as 'selfcom' signal outputted by the DRAM state controller 800. The generator 600 is enabled by the selfref signal and then ouputs a clock signal (hereinafter, referred as 'ck' signal) of reference frequency, e.g., a frequency in about 1MHz. The frequency divider 500 outputs a signal after divides the ck signal. The self-refresh mode controller 100 ouputs a self-refresh operation signal (hereinafter, referred as 'selfreq' signal) which represents a timing for starting the self-refresh operation using the ouput of the frequency divider 500. The sense-amplifier controller 900 outputs a sense-amplifier enable signal (hereinafter, referred as 'SG' signal) after receiving the selfreq signal. The self-refresh termination controller 950 outputs a self-refresh termination signal (hereinafter, referred as 'sensdly'

signal) for finishing the self-refresh operation at time that a sense-amplifier completes sensing and amplifying the data in the bit line after receiving the SG signal. The cell area 400 has a plurality of cell units. The cell controller 200 controls the refresh operation of the cell area 400 by the selfreq signal and the sensdly signal. The power supply division 300 supplies a power to the cell area 400 and the cell controller 200.

On page 12, paragraph beginning on line 24, lines 24-25,

Fig. 6 is a circuit diagram of ~~a~~ the low-power controller 300' shown in Fig. 5.

On page 14, paragraph beginning on line 17, line 19,

As shown, the high-voltage generating pump 323 includes two inverters IN9 and IN10 buffering an output signal OSC of the generator 322; a first diode D1 connected to the supply voltage VDD; a first capacitor C1 connected between an output of the diode D1 and an output of the inverter IN10; a second diodes D2 connected to an output of the diode D1; and a second capacitor C2 connected to an output of the diode D2. Herein, a high-voltage VPP outputted from the capacitor flows through the high-voltage sensor 321 and the internal circuit.

On page 15, paragraph beginning on line 8, lines 9-10,

Fig. 11 is a circuit diagram of a delay block shown in Fig. 4. Herein, the delay unit includes several serial-connected inverters, i.e., IN11 to IN20.

On page 20, paragraph beginning on line 3, lines 3-9,

In Fig. 14, there are described two cell arrays 55 and ~~56~~59, a sense-amplifier division 57 for sensing and amplifying a voltage of the bit line connected to the cell arrays 55 and ~~56~~59, switching transistors 56 and 58 for connecting or disconnecting the sense-amplifier division 57 to the cell array in response to a first bit isolation signal BISH1 and a second isolation signal BISL1, and a sense-amplifier connection control division for controlling the switching transistors 56 and 58.